carbon-rich environment. This C is carbidic in nature.

Annealing the sample at 500 °C for 1 h in a 10^{-9}-Torr vacuum results in migration of the S and O to the near-surface region. The S lies in the outermost atomic layer with the O lying in the subsurface region. Most of the O desorbs, and the C and O concentrations are low throughout the bulk of the film.

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Deep Anisotropic Etching of Tapered Channels in (110)-Oriented Silicon

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A 50 wt % potassium hydroxide and deionized water anisotropic etchant was utilized to isothermally (85 °C) etch a staggered array of deep (290 μm), 5-μm wide, closely spaced (20.4 μm), smooth-walled, tapered channels in (110)-oriented silicon wafers. A quantitative relationship that specifies the channel length as a function of the channel width and depth is developed. A buffered hydrofluoric acid isotropic etchant was employed to sharply point the top edges of the channel walls.

Introduction

Single-crystal silicon has revolutionized technology during the past 20 years comparable to that attributed to steel in the midst of the industrial revolution. The most prominent technological contribution of silicon has been the emergence of the integrated circuit (IC) electronics industry.[1] In addition to its favorable and comprehensively documented electrical properties, silicon possesses exemplary mechanical and thermal characteristics. Silicon commands a substantially higher stiffness-to-weight ratio compared to most common materials, including steel and titanium.[2] In addition, silicon is a good conductor of heat, comparable with aluminum at room temperature; and similar to diamond, its thermal conductivity increases with decreasing temperature.[2] As a result of the mechanical characteristics being coupled with the precise IC microfabrication technology that was developed for patterning and etching silicon, a host of novel microelectronic, electrochemical, electromechanical, and micromechanical devices and components have recently emerged. Several extensive reviews of the basic processes and structures are available in the literature.[2-9] It is now common practice to refer to the fabrication of sophisticated three-dimensional micromechanical structures from silicon as micromachining.[2-5]

The anisotropic etching mechanism of silicon has been attributed to the crystallographic properties of the various planes, and it has been experimentally verified to be particularly sensitive to the atomic packing density. Accordingly, the relative etch rate decreases as the atomic packing density increases. Since the packing density of silicon atoms is substantially greater in the ⟨111⟩ direction compared to the ⟨100⟩ or ⟨110⟩ directions, the {111} planes etch much slower compared to either the {100} or {110} planes.[6-9]

There are three common anisotropic etchants for (100)- and (110)-oriented silicon. The most intensively studied etchant is the potassium hydroxide–water (KOH) system. For example, a 50 wt % mixture of each component at 85 °C exhibits an etch rate of 1.43 μm/min for the (100) plane, 0.6 μm/min for the (110) plane, and 0.007 μm/min for the (111) plane. Correspondingly, the differential etch rates are approximately 200/1 for the (100)/(111) planes and 86/1 for the (110)/(111) planes.[5,10-15] On the other hand, the ethylenediamine–pyrocatechol–water (EDP) etchant (typically, 750 mL–120 g–240 mL at 115 °C) manifests an etch rate of 1.25 μm/min for the (100) plane and a 35/1 differential etch rate for the (100)/(111) planes.[16-26] Finally and less thoroughly investigated is the hydrazine–

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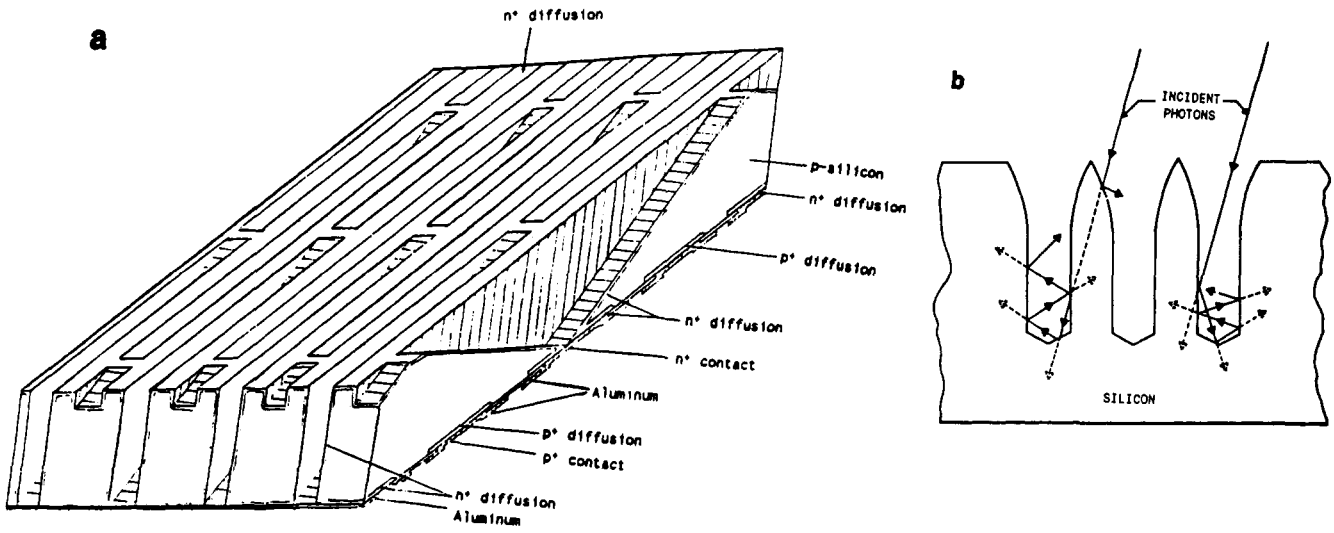

Figure 1. (a) Arrangement of the rectangular-shaped, tapered channels used in a back-contact, vertical junction silicon solar cell design. (b) Cross-sectional view depicting the principle of multiple reflections utilized to achieve a "blackbody" cavity when the top edges of the channels are "pointed" with an isotropic polishing etchant.

water etchant. A 50 vol % mixture of each component at 118 °C in a nitrogen environment exhibits an etch rate of 3 μm/min for the (100) plane and a 16/1 differential etch rate for the (100)/(111) planes.[27-31] Reviews of the chemical kinetics associated with these etchants have recently been published.[3,14,31]

Because of its superior differential etch rates and lower toxicity, the KOH anisotropic etchant was utilized in this investigation to deeply etch tapered channels in (110)-oriented silicon. The resulting array consists of staggered, rectangular-shaped channels that have two long-length parallel vertical walls and two narrow-width tapered walls that converge to form a narrow slit on the backside of the host wafer. This structure will be utilized in the future to implement a back-contact, vertical-junction solar cell. This particular three-dimensional pattern evolved from the solar cell design requirement to create a mechanically robust structure that functions as a "blackbody" absorption cavity. Figure 1a illustrates the channel configuration, and Figure 1b depicts the principle of multiple reflection and the near-total absorption that is anticipated when the channel's long parallel vertical wall edges are "pointed" with a conventional silicon planar etch. The merit of the vertical-junction feature of the proposed solar cell design has also been discussed by Smeltzer.[32] By extension, it is envisaged that this structure could also serve other applications, such as an in situ IC passive heat radiator,[33] thereby taking advantage of the favorable thermal conductance and mechanical strength properties of silicon.

Quantitative Analysis

A critical issue concerning the tapered channel structure investigated in this study included a requirement to determine the channel's width and length, such that it just etched through the backside of a (110)-oriented silicon wafer and manifested itself as a narrow slit. According to the literature, the internal walls of long grooves etched in (110)-oriented silicon consist only of {111} planes.[8] Since a quantitative relationship for the channel geometry fabricated in this investigation was not available in the literature, an equation relating the channel depth (d), length (L), and width (W) was developed. The resulting calculation has been experimentally verified.

The tapered channel geometry of interest is illustrated in Figure 2. The angle (ϕ) between any two of the channel's intersecting planes with Miller indices ($h_1k_1l_1$) and ($h_2k_2l_2$) can be calculated by using[34]

$$\phi = \cos^{-1}\left\{\frac{h_1h_2 + k_1k_2 + l_1l_2}{[(h_1^2 + k_1^2 + l_1^2)(h_2^2 + k_2^2 + l_2^2)]^{1/2}}\right\}$$

From Figure 2

$$d = [(L + L_1)/2] \tan \theta_1 \quad (1)$$

where

$$L_1 = W/\tan \theta_2 \quad (2)$$

Substituting eq 2 into eq 1 and rearranging yield

$$d = (L/2) \tan \theta_1 + (W \tan \theta_1)/(2 \tan \theta_2) \quad (3)$$

For eq 3 to be useful, θ_1 and θ_2 must be determined. As illustrated in Figure 2, these two angles (θ_1 and θ_2) do not describe the intersection of two specific crystallographic planes but are instead located between the lines that result

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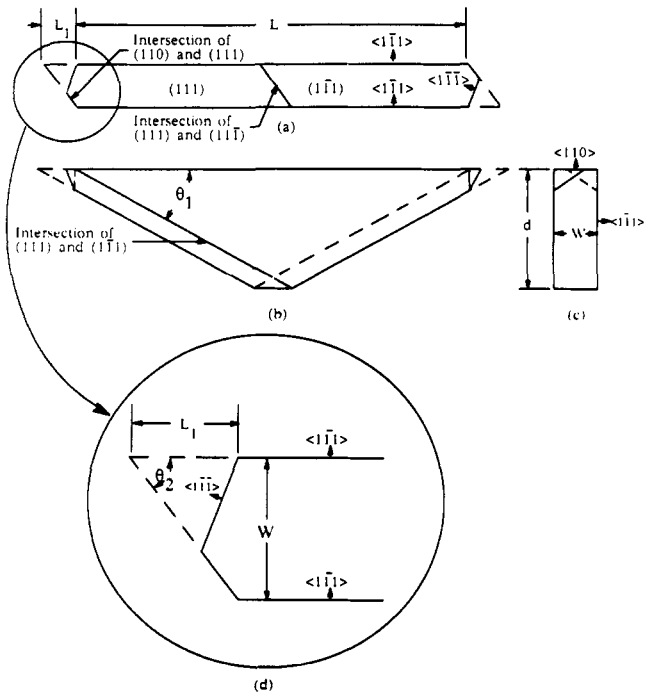

Figure 2. Tapered channel geometry utilized to determine the quantitative relationship between the length (L), depth (d), and width (W): (a) top view; (b) side view; (c) end view; (d) enlarged top view depicting the end of a channel.

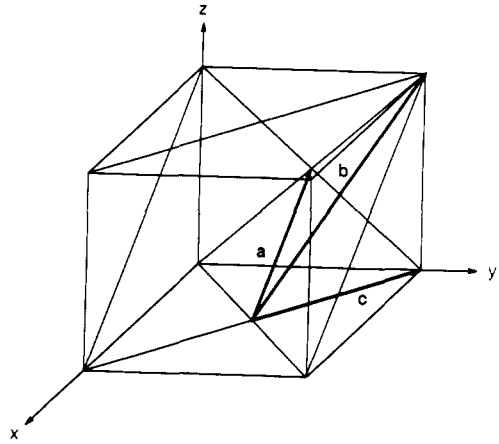

Figure 3. Vectors representing the lines formed by the intersection of two specific Miller indexed planes.

when specific sets of planes intersect. That is, angle θ_1 is located between the line formed by the intersection of the (110) and (1$\underline{1}$1) planes and the line formed by the intersection of the (111) and (1$\underline{1}$1) planes. Similarly, angle θ_2 is located between the line formed by the intersection of the (110) and (111) planes and the line formed by the intersection of the (110) and (1$\underline{1}$1) planes. From Figure 3, vectors **a**, **b**, and **c** can be utilized to describe the lines that are formed by the intersections of these Miller indexed planes, that is

a = intersection of the (111) and (1$\underline{1}$1) planes = $-0.5\mathbf{i} + 0.5\mathbf{k}$

b = intersection of the (110) and (1$\underline{1}$1) planes = $-0.5\mathbf{i} + 0.5\mathbf{j} + \mathbf{k}$

c = intersection of the (110) and (111) planes = $-0.5\mathbf{i} + 0.5\mathbf{j}$

The corresponding angles (θ_1 and θ_2) between these vectors can be calculated by using the vector dot product relationship; that is

$$\theta_1 = \cos^{-1}\left[\frac{(\mathbf{a}\cdot\mathbf{b})}{(|\mathbf{a}||\mathbf{b}|)}\right] = 30°$$

$$\theta_2 = \cos^{-1}\left[\frac{(\mathbf{b}\cdot\mathbf{c})}{(|\mathbf{b}||\mathbf{c}|)}\right] = 54.73°$$

Substituting the numerical values for θ_1 and θ_2 into eq 3 and solving for the channel length (L) in terms of its depth (d) and width (W) yield the following quantitative result:

$$L = 2d(3^{1/2}) - (W/2^{1/2}) \quad (4)$$

In practice, since the thickness of a silicon wafer (that is, the channel's depth (d)) can be precisely measured (on the order of 0.1 μm), eq 4 can be used to calculate the channel length (L) for a specific value of its width (W).

As a point of reference, Ammar,[9] Kendall,[12] and Allen[14] report a similar quantitative relationship for a much simpler rectangular-shaped channel structure. In terms of the channel variables used in eq 4, their result is

$$L = 2d(3^{1/2}) - 3(2^{1/2})W/4 \quad (5)$$

For the channel width (W) and depth (d) dimensions examined in this investigation, eq 5 predicts the channel's length (L) to within 1 μm when compared to the exact calculation given by eq 4.

Experimental Section

Materials and Instrumentation. The 2-in.-diameter (110)-oriented silicon wafers utilized in this investigation were Czochralski grown, polished on both surfaces, boron doped, had an average resistivity of 2.5 Ω·cm, and were individually inspected to verify that the reference orientation flat was accurately positioned to within 0.5° (Virginia Semiconductor, Fredericksburg, VA). The wafers were initially cleansed of organic and inorganic contaminants by using the IC standard process;[35] this procedure was also implemented as needed to complete the photolithographic and oxidation processes. The thickness of the wafers spanned 290–293 μm. Since a common wafer thickness (d) was critical to this investigation, the wafers were thinned to a uniform thickness of 290 μm by using the standard isotropic polishing etchant composed of HF:HNO_3:CH_3COOH (2:15:5).[36] This isotropic polishing solution was also utilized in the final processing step to "point" the long vertical walls in the tapered channel structure.

To achieve the deeply etched tapered channel structure, the results reported by Kendall[5,12] for the KOH etchant were utilized. Since the etch rate in the ⟨110⟩ direction should be as large as possible relative to that in the ⟨111⟩ direction, a 50 wt % KOH solution thermostated at 85 °C was utilized. The isothermal etch conditions (85 °C) were achieved with a Lufran Superbowl II reflux etching system (Lufran, Inc., Macedonia, OH). A 1-L etch solution volume was prepared from semiconductor grade (99.99%) KOH pellets (Aldrich Chemical Co., Milwaukee, WI) that were dissolved in deionized water. The vessel for the etchant was made of Teflon, and the wafers were transported in a standard polypropylene holder.

To precisely control the dimensions of the tapered channels, a high-quality silicon dioxide mask layer was thermally grown at 900 °C under steam conditions. From Kendall's findings,[5,12] a 1.3-μm-thick oxide mask is reported to be sufficient to satisfy this need. For an added margin of safety, a 1.5-μm-thick silicon dioxide mask was utilized. Conventional negative photoresist

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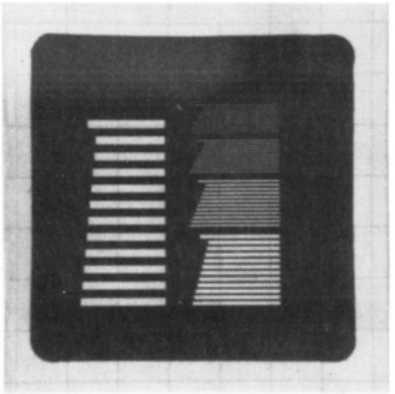

Figure 4. Reticle design consisting of five sets of test patterns, each of which possesses a common width (W). The element in the uppermost position in each set represents the calculated theoretical length (L). The other elements in a given set represent incremental ±20-μm-length variations. The left-most set corresponds to the 100-μm test channel width (W), the uppermost set on the right corresponds to the 5-μm width, and the intermediate sets correspond to the widths summarized in Table I. This reticle was stepped-and-repeated to produce an 8 × 8 array photomask.

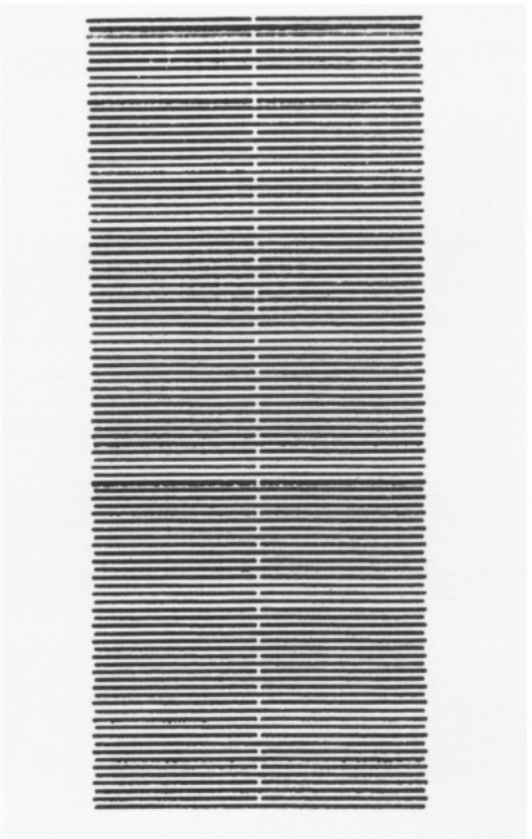

Figure 5. Fundamental reticle pattern for the step-and-repeat generation of the tapered channel structure.

Table I. Theoretical Length (L) of a Channel Given a Specific Width (W) and Thickness (d = 300 μm)

length, μm	width, μm	length, μm	width, μm
1036	5	1004	50
1032	10	969	100
1022	25		

lithography followed by an isotropic oxide etch using a buffered hydrofluoric acid solution (NH_4OH:HF,6:1) was utilized to mask the channel geometry on the wafer's surface. To ensure exact replication of the photomask image, a precision mask alignment instrument (Karl Suss America, Inc., Model MJB3-UV300, Waterbury Center, VT) was used to align the image to within 0.1° relative to the wafer's reference orientation flat.

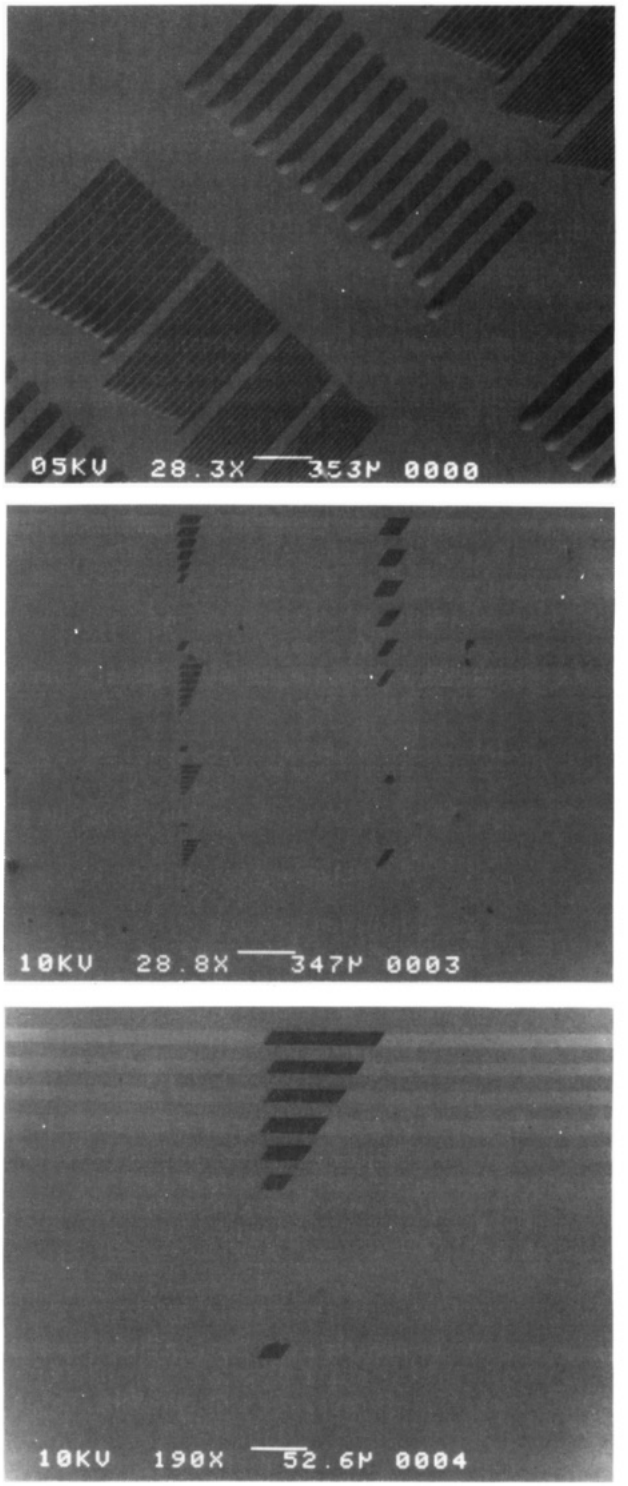

Figure 6. (a) Front surface of a silicon wafer that depicts the test channel pattern after completion of the anisotropic etch process. (b) Back surface of the same silicon wafer showing one complete pattern of the etched slits. (c) Enlarged view of the etched slits associated with the 5-μm-wide test channel pattern.

Test Channel Photomask Design. To verify eq 4, a test channel pattern and photolithographic mask was designed. For an assumed wafer thickness (d) of 300 μm, a set of five channel widths (W) were specified (5, 10, 25, 50, and 100 μm), and finally, the theoretical length (L) for each channel was calculated. The results are summarized in Table I. In practice, sets of channel structures, grouped by their common width (W), were created by incrementing the theoretical channel length by an integral

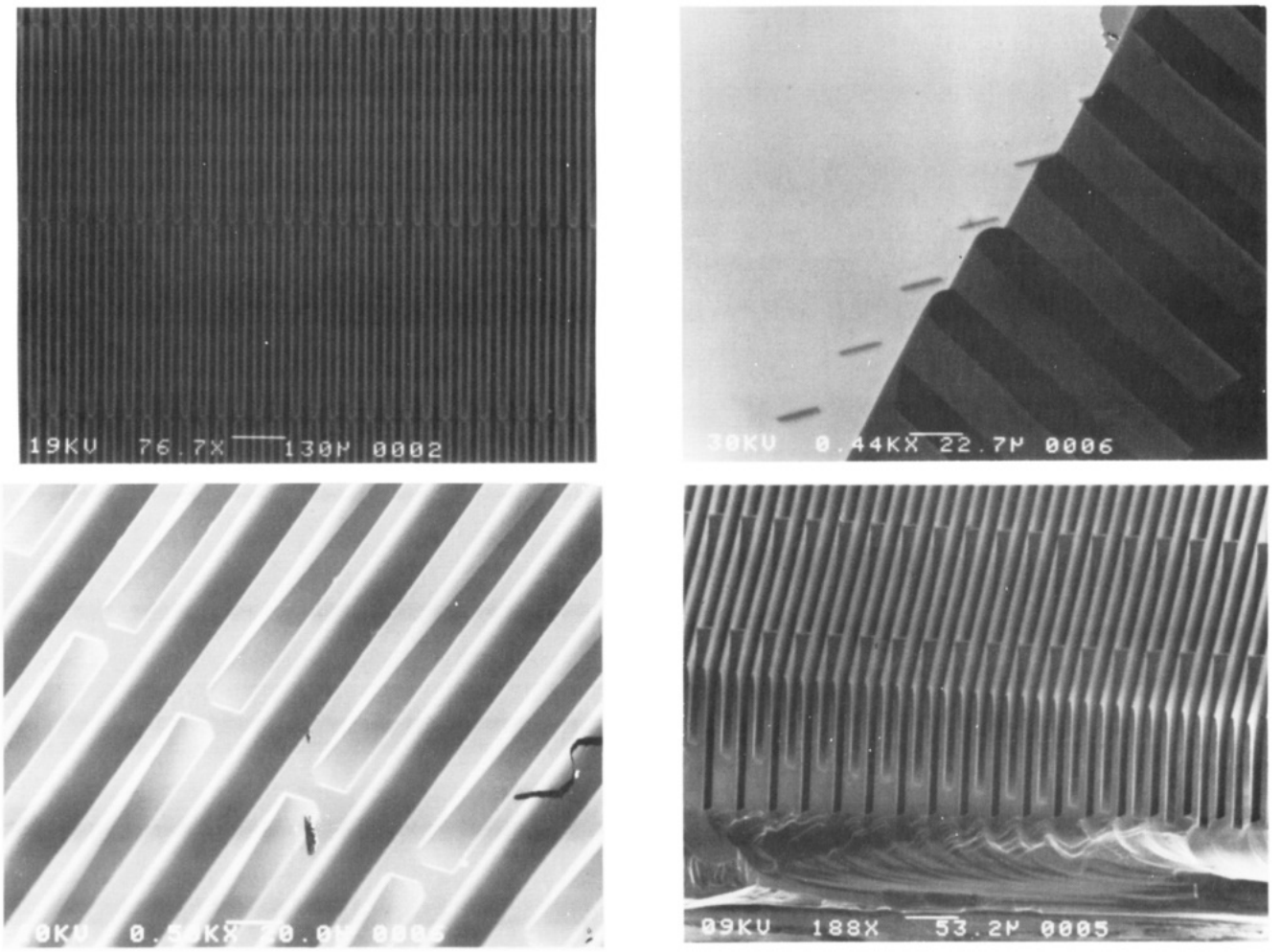

Figure 7. Anisotropically etched tapered channel structure: (a) top view showing the staggered channel geometry after the silicon dioxide mask was removed; (b) top view (tilted) showing the 30° angle (taper) associated with the end walls after the silicon dioxide mask was removed; (c) cross-sectional view showing the etched channels and the backside slits (the silicon dioxide mask layer is present); (d) cross-sectional view showing an array of staggered channels and the wafer's upper surface.

multiple of ±20 μm. As illustrated in Figure 4, each test channel set possessed 12 elements whose length varied. The uppermost (or first) element in each set corresponds to the calculated theoretical length, and the other elements represent the incremental ±20-μm length variations. To enhance the observability of an etched slit on the wafer's backside, the wafers were thinned to a thickness of 290 μm.

Tapered Channel Photomask Design. To realize an array of mechanically robust tapered channels etched into a 290-μm-thick (110)-oriented silicon wafer, a staggered arrangement of channels was designed. Considering the resolution of the laboratory photolithographic system (4 μm), the precision of the associated step-and-repeat camera system, and the errors associated with aligning a photomask with respect to the wafer's reference orientation flat (must be aligned to within 0.1° (ref 12, 16, 32)), the following conservative channel dimensions were utilized: 1000-μm channel length (L), 5-μm channel width (W), a 20.4-μm side-to-side channel separation, and a 16-μm end-to-end channel separation. The fundamental staggered channel pattern illustrated in Figure 5 was stepped-and-repeated to generate a square cell whose length measured 10 160 μm. Five well-separated cells were etched into the surface of each host wafer.

Results and Discussion

Test Channel Etch. Figure 6a depicts one complete test channel pattern that was anisotropically etched into the surface of a wafer. Figure 6b depicts the backside of the same wafer. The grooves that etched through the wafer were only those which were longer than or equal to the calculated theoretical length (L). The slit widths also scale to the channel widths summarized in Table I, which implies that the channel's vertical walls not only are parallel but are also perpendicular to the wafer's upper and lower surfaces. As shown in Figure 6b,c, the slit lengths are longer than anticipated, but this feature is attributable to the fact that the theoretical calculations were based upon an assumed 300-μm-thick wafer, while the actual wafers were slightly less than 290-μm thick (accounting for the silicon consumed during thermal oxidation). Consequently, the wafer thickness margin of error (10 μm) intentionally incorporated into this investigation to produce clearly discernible etched-through slits was sufficiently small to prevent a channel whose length was 20 μm less than the theoretical value from etching through the wafer's backside. Thus, eq 4 can be utilized as a design tool for generating etched-through, tapered channels in (110)-oriented silicon.

Tapered Channel Etch. Figure 7a depicts the wafer's surface as a result of implementing the anisotropic etch process for the staggered, tapered channel pattern. Figure 7b shows an enlarged view of the wafer's surface and the 30° angle (taper) associated with the end walls. The 5-μm-wide channels have vertically etched side walls, and the texture of all the etched surfaces appears smooth and uniform. In addition, the "characteristic shape" associated with the ends of a channel (Figure 2) are clearly discernible. Figure 7c depicts a cross-sectional view of the

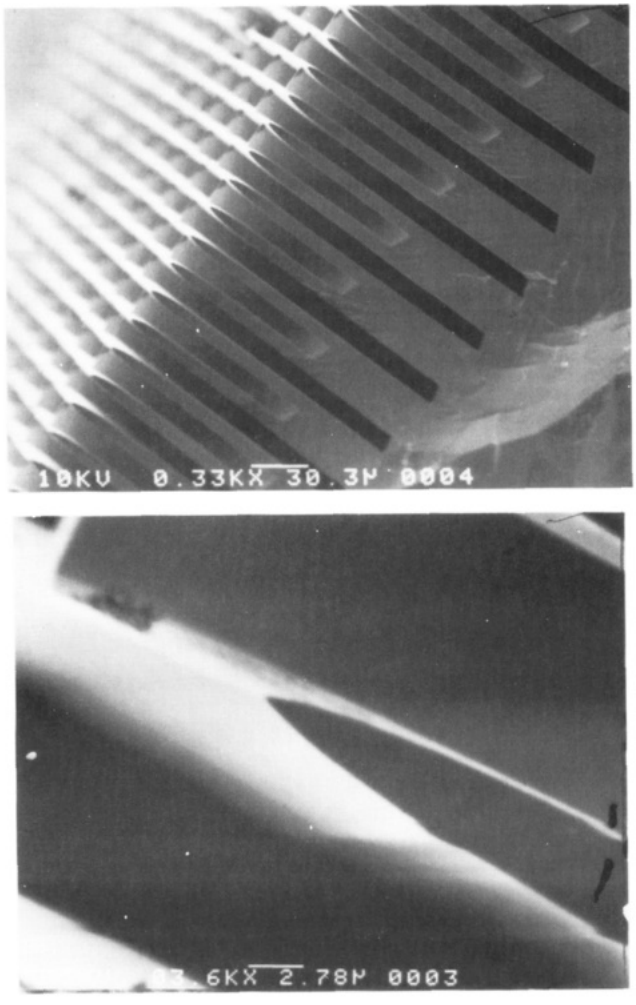

Figure 8. Isotropically etched pointed walls of the tapered channel structure: (a) cross-sectional view showing the "pointed" edges of the channel walls; (b) magnified view of a discrete, sharply pointed wall.

channels and the narrow slits that etched through the backside of the oxide-covered wafer. The formation of the slit feature results because all the channel walls are {111} planes, and for practical purposes, the etch process terminates. Figure 7d is a physical manifestation of the drawing shown in Figure 1, and its was produced by scribing and breaking an etched wafer. For the perspective illustrated, the uniformity and precision of the etch process are evident.

The isothermal (85 °C) etch process associated with the 50 wt % solution of potassium hydroxide and deionized water required an average duration of 180 min to attain completion (observation of the slits on the wafer's backside). Etching slightly longer than 180 min is not a critical problem, since the etching of silicon is very slow once the channel's {111} planes intersect on the wafer's backside. However, etching for periods of time that are much longer than necessary should be avoided because the protective silicon dioxide mask continues to etch, and the channel walls will gradually become thinner and thus weaken the structure.

The anisotropic etchant concentration and processing temperature contributed to produce excellent etch depth uniformity and smooth channel side walls. According to the literature,[5,12] the etch rate at 85 °C for a 50 wt % potassium hydroxide and deionized water solution is approximately 1.43 μm/min; the calculated average etch rate was 1.6 μm/min. A stylus profilometer was utilized with a control wafer to establish a silicon dioxide etch rate of 0.007 μm/min; the literature[5,12] reports a value of 0.006 μm/min.

The final version of the tapered channel structure was realized by isotropically etching the top edges of the channel walls to "point" them (Figure 1b)). A 5-min immersion in the buffered hydrofluoric acid etchant (HF:HNO_3:CH_3COOH, 2:15:5) produced the sharply pointed side walls depicted in Figure 8.

Conclusion

A 50 wt % solution of potassium hydroxide and deionized water can be utilized to isothermally (85 °C) etch deep (290 μm), smooth-walled, tapered channels in (110)-oriented silicon. Channel widths as small as 5 μm can be realized. If the pattern to be etched is carefully aligned with respect to the wafer's reference flat (on the order of ±0.1°), channel side-to-side spacings as small as 20.4 μm can be etched. The length (L) of a channel can be calculated from the quantitative relationship developed in this paper as a function of the channel's width (W) and depth (d). A buffered hydrofluoric acid isotropic etchant can also be utilized in the micromachining process to "point" the top edges of the channel walls. The synergistic combination of isotropic and anisotropic etching processes has been utilized to fabricate a "blackbody" absorption cavity for a novel solar cell design, and this structure might also be applied as an in situ passive heat radiator for integrated circuits or used in related applications.

Registry No. Si, 7440-21-3.